Assignment 14

Flip Flop

Introduction

We will build a flip flop with enable and clear bits. The flip flop will store one bit of data. The enable signal is a proxy for the clock. When it is 1 (rising clock), the data bit will be written. When it is 0 (falling clock), the data bit will be maintained in its current state. When the clear bit is set, the stored data bit will be cleared (set to 0) regardless of the states of the input date and the enable signal.

The Circuit

Begin by building the basic SR latch. Replace the upper NOR-gate with a 3-way NOR-gate. Reconnect the original two inputs to the first and third inputs of the 3-way gate. The middle input should be connected to the clear bit. The Q output bit should be 1 when the S input bit is 1 and 0 when the R input bit is 1. In either case, when the clear bit is set, it should clear the Q output bit. (We do not care about the $\overline{Q}$ output.) Test this circuit.

Next, use the SR latch to build a D latch with three input bits: the data bit, the enable bit, and the clear bit. When the enable bit is set, the data bit should be written to the Q output bit. When the clear bit is set, then Q should be 0 no matter the states of the data bit or the enable bit. Test this circuit.

Finally, using two D latches, build a flip flop. The enable bit should now be labeled as the clock. Test this circuit.

Due Date

This assignment will not be collected, but it will be the starting point of Assignment 15, which will be to build a 32-bit register.